

Heterogeneous Programmable Logic Resources," filed March 31, 2003, under Attorney Docket
10/404,680
~~No. PA2586~~, which is hereby incorporated by reference.

Change(s) applied
to document,

/P.A.P./
4/25/2011

- [00038] The processing element 220 is a processor configured to execute applications. The processing element 220 includes a standard or native instruction set that provides a set of instructions that the processor element 220 is designed to recognize and execute. These standard instructions are hard-coded into the silicon and cannot be modified. One example of the processing element 220 is an Xtensa processor, from Tensilica, Inc., of Santa Clara, California. One example of the processing element 220 is also described in U.S. Application Serial Number 10/404,706 filed on March 31, 2003 and titled "Reconfigurable Instruction Set Computing."
- [00039] The processing element 220 is coupled to an instruction cache 222 and a data cache 224. The instruction cache 222 is a cache configured to store instructions for execution either permanently or temporarily. The data cache 224 is a cache configured to store data either permanently or temporarily. The local data RAM 230 is also coupled to the processing element 220.
- [00040] The local data RAM 230 is any local memory for the processing element 220 that is configured to store data. In one embodiment, an exemplary size of the local data RAM 230 is 128 kB or 256 kB. The local data RAM 230 can operate as a buffer for buffering incoming and outgoing messages in accordance with a "channel" implementation. In some embodiments, the local data RAM 230 is either a single-ported or dual-ported RAM.
- [00041] The processor network interface 240 is coupled to the processing element 220. The processor network interface 240 operates as a conduit between the processing element 220 and the network of the array of processor nodes 140. The processor network interface 240 is a communication interface configured to receive data from the processing element 220 and transfer the data to the processor network switch 250 for transport over the network of the array of processor nodes 140. When the processor network interface 240 receives data through the